IN THE CLAIMS:

Please cancel claim 2 and amend claims 1, 3, 4 and 5 to read as follows:

1. (Currently Amended) In a microprocessor having a program control and a plurality of circuit components comprising registers, arithmetic logic units, memory and input/output circuits, the improvement wherein said plurality of components are interconnected ~~in a manner which allows connection between some of the components to be varied under said program control~~ on a grid and wherein each of said plurality of components can be switched under program control to be connected to a predetermined selection of one or more of said plurality of components to route data through said grid for processing by said predetermined selection of one or more of said plurality of components.

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2. Canceled.

3. (Currently Amended) The microprocessor as claimed in claim ~~2~~ 1, further ~~including~~ comprising a grid connector

which includes logic for interconnecting a predetermined one or more of said plurality of components with one or more other components of said plurality of components ~~on~~ to said grid.

B2 4. (Currently Amended) The microprocessor as claimed in claim 1, ~~wherein said plurality of components are interconnected on a grid such that each of said plurality of components can be switched under said program control to be connected to a predetermined selection of one or more of said plurality of components, and~~ further comprising an instruction set decoder for interpreting the instruction set of said microprocessor into timed signals to said components, a clock for timing operations of said microprocessor and a grid connector which provides logic for interconnecting a predetermined one or more of said plurality of components with one or more other components of said plurality of components ~~on~~ to said grid.

5. (Currently Amended) The microprocessor as claimed in claim ~~2~~ 1, further ~~including~~ comprising at least one further grid of a plurality of ~~interconnected~~ further components

B2 ~~comprising~~ which are selected from registers, arithmetic logic units, memory, and input/output circuits, and wherein at least a part of said grid is coupled to at least a part of said at least one further grid.
